REMARKS

Claims 1-16 were pending. Claims 1 and 12 have been amended for clarity.

The Examiner states that non-patent literature cited in Applicant's Information Disclosure Statement filed December 8, 2003 has not been considered because copies of the documents were not enclosed. As noted by applicant's representative in a prior telephone call, the documents were submitted to the Patent Office in prior application no. 10/121,790 filed April 10, 2002 and relied upon in this application for an earlier filing date under 35 U.S.C. § 120. Consideration of the non-patent literature respectfully is requested. A copy of the previously-submitted Form PTO 1449 listing the non-patent literature is enclosed for the convenience of the Examiner.

The Examiner requires that the Form PTO 1449 list U.S. Patent No. 5,177,567 and U.S. Patent No. 6,337,266. Applicant notes that U.S. Pat. No. 5,177,567 is listed on page 2 of the attached copy of the IDS submitted December 8, 2003, and that the Examiner has indicated that he already considered the patent. Enclosed is an IDS which includes the '266 patent.

The Examiner objects to claims 1 and 12 because of informalities. Claims 1 and 12 have been amended to address the Examiner's concerns.

Claims 12 and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pub. No. 2003/0038301 to Moore. The rejection of these claims is traversed.

Claim 12 recites a method of forming a programmable conductor memory cell including "forming a cathode," and "forming a glass electrolyte element in contact with the cathode and having a sidewall edge." The method also includes "forming an insulating layer over the glass electrolyte element and covering the sidewall edge," and "forming an opening in the insulating layer, to expose a surface of the glass electrolyte element without exposing the sidewall edge." In addition, the method includes "depositing a layer of

conducting material into the opening to contact only the central portion of the surface of the glass electrolyte element, thus forming an anode."

The reference to Moore discloses a stacked pair of memory cells having a common anode. The anode is formed in an opening that exposes the sidewall edge of the glass electrolyte element. The Moore reference does not anticipate the present invention recited in claim 12, which recites forming a programmable conductor memory cell by a method that includes "forming a cathode," "forming a glass electrolyte element in contact with the cathode and having a sidewall edge," "forming an insulating layer over the glass electrolyte element and covering the sidewall edge," and "forming an opening in the insulating layer, to expose a surface of the glass electrolyte element *without exposing the sidewall edge.*" In addition, the reference to Moore does not anticipate the method of claim 12 which includes "depositing a layer of conducting material into the opening to contact only the central portion of the surface of the glass electrolyte element, thus forming an anode." . Claim 12 and its dependent claims 13-16 are submitted as patentable over the cited reference to Moore.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: April 16, 2004

Respectfully submitted,

By_____

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Attachment: Copy of Form PTO 1449 submitted December 8, 2003